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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/816,311 | 03/31/2004 | Nick Lindert | 42P18257 | 9112 |
| 7590 | 04/18/2005 | | EXAMINER | |
| Michael A. Bernadicou BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP Seventh Floor 12400 Wilshire Boulevard Los Angeles, CA 90025 | | | NGUYEN, JOSEPH H | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2815 | |
| DATE MAILED: 04/18/2005 | | | | |

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | |
|------------------------------|-----------------|----------------|
| Office Action Summary | Application No. | Applicant(s) |
| | 10/816,311 | LINDERT ET AL. |
| | Examiner | Art Unit |
| | Joseph Nguyen | 2815 |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 28 March 2005.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-42 is/are pending in the application.
 4a) Of the above claim(s) 20-42 is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-10 and 12-19 is/are rejected.
 7) Claim(s) 11 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 31 March 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

| | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

Applicant's election of claims 1-19 in the reply filed on 3/28/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Objections

Claims 3, 10 and 11 are objected to because of the following informalities: --and then-- in line 2 of claim 3 should be corrected to read "than", and --semiconductor body- - in lines 7 and 10 of claim 10, and in lines 2-3 of claim 11 should be corrected to read "silicon germanium body". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 10, 12-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Sugiyama et al. (US 2003/0227036 A1)

Regarding claim 1, Sugiyama et al. discloses on figure 2 a semiconductor device comprising a semiconductor body 30 on a semiconductor substrate 10, said semiconductor body having a top surface and laterally opposite sidewalls; a semiconductor capping layer 40 formed on the top surface and on the sidewalls of said semiconductor body; a gate dielectric layer 70 formed on said semiconductor capping layer on said top surface and on said sidewalls of said semiconductor body; a gate electrode 80 having a pair of laterally opposite sidewalls formed on and around said gate dielectric layer; and a pair of source/drain regions 50, 60 formed in said semiconductor body on opposite sides of said gate electrode.

The term "capping layer" is merely a label. Element 40 is considered "capping layer" since it constitutes a similar structure and function as the claimed capping layer herein.

Regarding claim 2, Sugiyama et al. discloses on figure 2 said capping layer 40 has a tensile stress. Applicant teaches, "a single crystalline silicon film formed on a silicon germanium alloy semiconductor body 208 will cause the single crystalline silicon film to have a tensile stress" (para [0017] of the instant application). Sugiyama teaches that the capping layer 40 is a silicon layer (para [0075]) formed on a silicon germanium alloy semiconductor body 30 (para [0075]). Therefore, the capping layer 40 inherently has a tensile stress.

Regarding claim 3, Sugiyama et al. discloses on figure 2 the semiconductor-capping layer has greater tensile stress on the sidewalls of the semiconductor body than on the top surface of the semiconductor body. Applicant teaches, "the silicon capping layer formed on the sidewalls 322 of the silicon germanium alloy will witness a substantial tensile stress and a lower but significant tensile strain on the top surface 319 of the silicon germanium alloy" (para [0043]). Sugiyama teaches that the capping layer 40 is a silicon layer (para [0075]) formed on a silicon germanium alloy semiconductor body 30 (para [0075]). Therefore, the semiconductor-capping layer inherently has greater tensile stress on the sidewalls of the semiconductor body than on the top surface of the semiconductor body.

Regarding claim 4, Sugiyama et al. discloses that the source/drain regions are n type conductivity (para [0066]).

Regarding claim 5, Sugiyama et al. discloses that the semiconductor substrate is a silicon substrate (para [0089]), wherein the semiconductor body is a silicon germanium alloy (para [0075]) and wherein the capping layer is a silicon film (para [0075]).

Regarding claim 10, Sugiyama et al. discloses on figure 2 a semiconductor device comprising a silicon germanium body 30 (para [0075]) on a silicon monocrystalline substrate (para [0089]), said silicon germanium body having a top surface and laterally opposite sidewalls; a silicon film 40 (para [0075]) formed on the top surface and on the sidewalls of said silicon germanium body; a gate dielectric layer 70 formed on said semiconductor capping layer on said top surface and on said sidewalls

of said semiconductor body; a gate electrode 80 having a pair of laterally opposite sidewalls formed on and around said gate dielectric layer; and a pair of source/drain regions 50, 60 formed in said semiconductor body on opposite sides of said gate electrode.

Regarding claim 12, Sugiyama et al. discloses on figure 2 the silicon film 40 has a thickness between 50-300A (para [0102]).

Regarding claim 13, Sugiyama et al. discloses on figure 2 the silicon germanium alloy comprises between 5-40% of germanium (para [0067]).

Regarding claim 14, Sugiyama et al. discloses on figure 22 the silicon germanium alloy comprises between 15-25% of germanium (para [0067]).

Regarding claim 15, Sugiyama et al. discloses that the source/drain regions are n type conductivity (para [0066]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6-8, 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugiyama et al., and further in view of Bohr et al.

Regarding claim 6, the difference between Sugiyama et al. and the claimed invention is the semiconductor-capping layer having a compressive stress. Applicant

teaches, "a single crystalline silicon capping layer 210 formed on a silicon carbon alloy semiconductor body 208 will cause the single crystalline silicon film 210 to have a compressive stress" (para [0017]). Sugiyama et al. teaches that the capping layer 40 is a silicon layer (para [0075]) formed on a silicon germanium (SiGe) alloy semiconductor body 30 (para [0075]), not on a silicon carbon (SiC) alloy body. However, Bohr et al. teaches that suitable silicon alloy materials may be used to cause strain include either SiGe or SiC (para [0024])). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sugiyama et al. by replacing SiGe body with SiC body, and therefore it will cause the capping layer to have a compressive stress for the purpose of increasing the performance of circuit devices on a substrate as taught by Bohr et al. (para [0002]).

Regarding claim 7, Sugiyama et al. and Bohr et al. together disclose the semiconductor-capping layer has a greater compressive stress on the sidewalls than on the top surface of the semiconductor body. Note that Sugiyama et al. and Bohr et al. together disclose a silicon capping layer is formed on a silicon carbon body, and it is assumed that a silicon capping layer formed on a silicon carbon body inherently has this feature.

Regarding claim 8, Sugiyama et al. discloses that the semiconductor substrate is a silicon substrate (para [0089]), wherein the capping layer is a silicon film (para [0075]). Sugiyama et al. and Bohr et al. (para [0024]) together disclose the semiconductor body comprises a silicon carbon alloy.

Regarding claim 16, the difference between Sugiyama et al. and the claimed invention is a silicon carbon (SiC) alloy body (see rejection of claim 10 above). Note that Sugiyama et al. teaches a silicon germanium (SiGe) body. However, Bohr et al. teaches that suitable silicon alloy materials may be used to cause strain include either SiGe or SiC (para [0024])). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sugiyama et al. by replacing SiGe body with SiC body, and therefore it will cause the capping layer to have a compressive stress for the purpose of increasing the performance of circuit devices on a substrate as taught by Bohr et al. (para [0002]).

Regarding claims 17 and 18, Sugiyama et al. discloses on figure 2 the silicon film 40 has a thickness between 50-300A (para [0102]).

Regarding claim 19, Sugiyama et al. disclose the source/drain regions are p type (para [0077]). Note that Sugiyama teaches this structure can be manufactured for both p and n channel MISFET's (para [0077]).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugiyama et al. and further in view of figure 1A of the acknowledged prior art (APA).

Regarding claim 9, the difference between Sugiyama et al. and the claimed invention is the semiconductor body comprising a silicon body. However, applicant disclosed on figure 1A of (APA) that the semiconductor body 102 is a silicon body. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sugiyama et al. by having the semiconductor

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body comprising a silicon body for the purpose of obtaining a better lattice matching between the capping layer and the body since they are both formed of silicon.

Allowable Subject Matter

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306 for regular communications.

JN
April 14, 2005

Tom Thomas
TOM THOMAS
SUPERVISORY PATENT EXAMINER